

**DATA PROCESSING APPARATUS WITH REGISTER FILE BYPASS****ABSTRACT OF THE DISCLOSURE**

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1 A data processing apparatus for increasing the speed of data  
2 transfer from one processor instruction to another processor  
3 instruction. First (78) and second (80) functional unit groups,  
4 each including a plurality of functional units, are connected to  
5 a register file (76) comprising a plurality of registers having  
6 corresponding register numbers. A comparator (181) receives an  
7 indication of the operand register number of a current  
8 instruction for a functional unit in the first functional unit  
9 group, and an indication of the destination register number of an  
10 immediately preceding instruction for the second functional unit  
11 group, and indicates whether the register numbers match. A  
12 register file bypass multiplexer (174) has a first input  
13 receiving data from the register corresponding to the operand  
14 register number of the current instruction, a second input  
15 (hotpath 172) connected to the output of the second functional  
16 unit group, and an output supplying an operand to the operand  
17 input of the first functional unit group. The multiplexer  
18 selects the data from the register corresponding to the operand  
19 number of the current instruction if the first comparator fails  
20 to indicate a match and selects the output of the second  
21 functional unit group if the comparator indicates a match. The  
22 first functional unit utilizes the output of the second  
23 functional unit group without waiting for the result to be stored  
24 in the register file, thus avoiding excess delay slots in the  
25 instruction pipeline.